AMENDMENTS IN THE CLAIMS:

The following is a complete listing of all claims in the application, with an indication of the status of each:

1   Claim 1 (Currently Amended). An integrated circuit including an embedded memory and
2   a built-in self-test arrangement including
3   means for storing test instructions ~~including means for~~ and discriminating a
4   ~~source of a test command for~~ between performing manufacturing level ~~and~~ or board
5   level testing and receiving test instructions provided from an external tester,
6   means for generating default test instructions **for performing manufacturing**
7   **level or board level testing**, and
8   means for supplying said default test instructions **for performing manufacturing**
9   **level or board level testing** to said means for storing test instructions,
10 **wherein said means for generating default test instructions includes an**
11 **initialization storage means**.

1   Claim 2 (Currently Canceled).

1   Claim 3 (Currently Amended). An integrated circuit as recited in claim ~~2~~ 1, wherein said
2   initialization storage means is a storage initialization module.

1   Claim 4 (Original). An integrated circuit as recited in claim 1, further including
2   means for activating said means for generating said default test instructions
3   responsive to an absence of test instructions from an external tester.

1   Claim 5 (Original). An integrated circuit as recited in claim 1, further including
2   means for controlling a test operation, wherein said means for controlling a test
3   operation includes means for supplying a control signal to an instruction storage
4   controller and further includes said means for storing said test instructions.

1   Claim 6 (Original). An integrated circuit as received in claim 5, further including

2   means for activating said means for generating said default test instructions when

3   only said control signal is supplied to said instruction storage controller.

1   Claim 7 (Original). An integrated circuit as recited in claim 1, wherein said means for

2   generating default test instructions includes a memory for storing said default test

3   instructions.

1   Claim 8 (Currently Amended). An electronic system including an integrated circuit

2   having a built-in self-test arrangement therein, said integrated circuit including

3   means for storing test instructions ~~including means for~~ and discriminating ~~a~~

4   ~~source of a test command for~~ between performing manufacturing level ~~and~~ or board

5   level testing and receiving test instructions provided from an external tester,

6   means for generating default test instructions **for performing manufacturing**

7   **level or board level testing** in absence of instructions from an external tester, and

8   means for supplying said default test instructions **for performing manufacturing**

9   **level or board level testing** to said means for storing test instructions**, wherein said**

10   **means for generating default test instructions includes an initialization storage**

11   **means.**

Claim 9 (Currently Canceled).

1   Claim 10 (Original). A system as recited in claim ~~9~~ **8**, wherein said initialization storage

2   means is a storage initialization module.

1   Claim 11 (Original). A system as recited in claim 8, further including

2   means for activating said means for generating said default test instructions

3   responsive to an absence of test instructions from an external tester.

1   Claim 12 (Currently Amended). ~~A method of performing system level tests on an~~

2   ~~electronic system including an integrated circuit having a built-in self-test (BIST)~~

3   ~~arrangement therein for performing manufacturing level and board level testing~~

4   ~~and including means for storing a test algorithm, said method comprising steps of~~

5   ~~discriminating a source of a test command;~~

6   ~~providing a system level test algorithm from said BIST arrangement in~~

7   ~~absence of instructions from an external tester;~~

8   ~~transferring said system level test algorithm to said means for storing a test~~

9   ~~algorithm in said BIST arrangement; and~~

10   ~~operating said BIST arrangement using said system level test algorithm~~

11   <u>A system as recited in claim 8, further including</u>

12   <u>means for controlling a test operation, wherein said means for controlling a</u>

13   <u>test operation includes means for supplying a control signal to an instruction</u>

14   <u>storage controller and further includes said means for storing said test instructions</u>.

1   Claim 13 (Original). A system as recited in claim 12, further including

2   means for activating said means for generating said default test instructions when

3   only said control signal is supplied to said instruction storage controller.

1   Claim 14 (Original). A system as recited in claim 12, wherein said control signal is

2   supplied from an external tester.

1   Claim 15 (Original). A system as recited in claim 12, wherein said control signal is

2   supplied from within said system.

1   Claim 16 (Original). A system as recited in claim 8, wherein said means for generating

2   default test instructions includes a memory for storing said default test instructions.

1   Claim 17 (Currently Amended). A method of performing system level tests on an

2   electronic system including an integrated circuit having a built-in self-test (BIST)

3   arrangement therein for performing manufacturing level ~~and~~ **or** board level testing and

4   including means for storing a test algorithm, said method comprising steps of

5   **discriminating a source of a test command,**

6   providing a system level test algorithm from said BIST arrangement **in absence of**

7   **instructions from an external tester,**

8   transferring said system level test algorithm to said means for storing a test

9   algorithm in said BIST arrangement, and

10   operating said BIST arrangement using said system level test algorithm.